
Section 46. Scalable Comparator Module

HIGHLIGHTS

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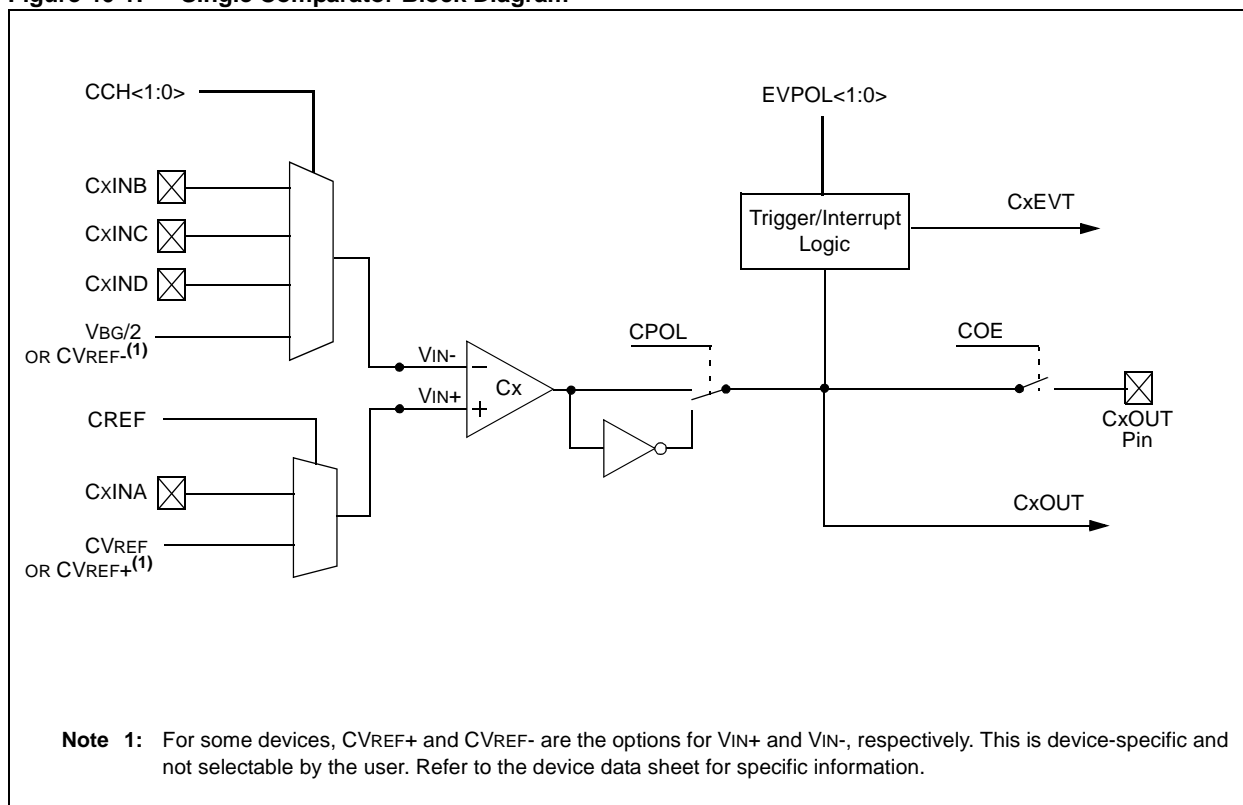
46.1 INTRODUCTION

The scalable comparator module is comprised of several identical analog comparator blocks, each complete with its own supporting input selectors and output logic. Each comparator can be configured in a variety of ways, independent of the other comparators. Inputs can be selected from four analog inputs multiplexed with I/O pins, external voltage references, and the on-chip voltage reference (see **Section 20. “Comparator Voltage Reference Module”**) or the on-chip band gap reference. A status register provides a single location to monitor all comparators simultaneously.

The block diagram for a single comparator is shown in Figure 46-1. Depending on the device family, the scalable comparator module may contain anywhere from two to six analog comparators; the most commonly used configuration contains three. Refer to the device data sheet for specific information.

Note: A comparator module with two analog comparators may also be the integrated dual comparator module, described in the Family Reference Manual chapter **“Dual Comparator Module”** (DS39710). Check the device data sheet to verify which comparator module is included in a particular device.

Figure 46-1: Single Comparator Block Diagram



46.1.1 Comparator Configuration

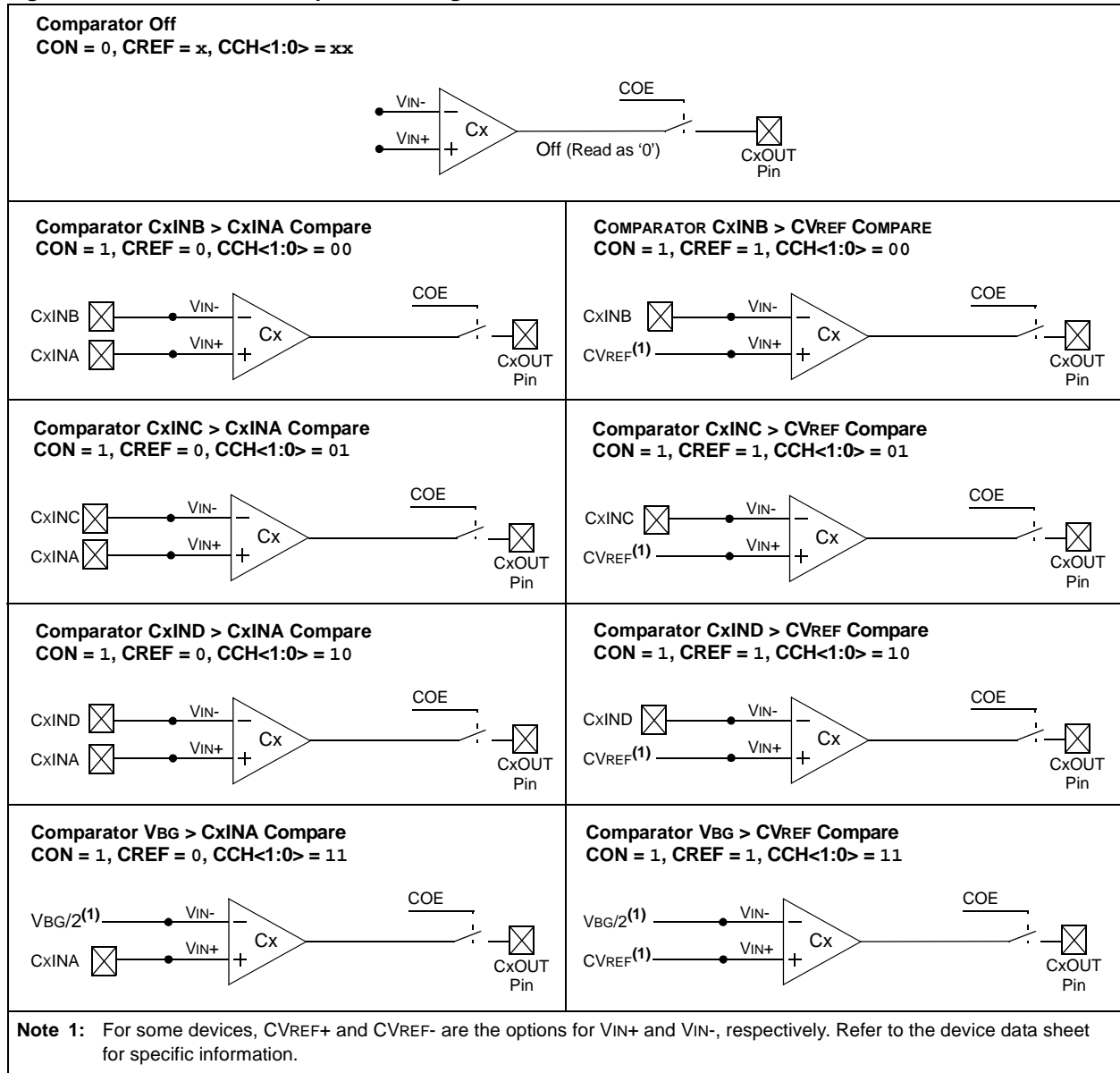
Each of the several comparators has complete control over its input selections, output inversion, output on I/O pin and event generation. The V_{IN-} input of each comparator can select from one of three I/O pins ($CxINB$, $CxINC$ or $CxIND$), while the V_{IN+} input of the comparator comes from the comparator voltage reference, or the positive I/O pin ($CxINA$ or $CVREF$). The comparators provide a common-mode voltage range which is nominally rail-to-rail, V_{SS} to V_{DD} . Refer to the particular data sheet for actual electrical specifications. The configuration options are shown in Figure 46-2.

The comparator also has four options to configure a separate event/trigger output based on changes of the comparator's output. Users can select from rising-edge, falling-edge, and all transitions.

If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay.

Note: Comparator interrupts should be disabled during a Comparator mode change; otherwise, a false interrupt may occur.

Figure 46-2: Individual Comparator Configurations



46.2 CONTROL REGISTER

The scalable comparator module uses several registers for configuration and control. Depending on the number of comparators, up to seven registers are implemented.

The CMxCON registers (Register 46-1) are used to configure the individual comparators. Each comparator uses its own individually-numbered CMCON register. The CON bit (CMxCON<15>) enables or disables the individual comparator. The COE bit (CMxCON<14>) enables the output of the comparator to appear on the corresponding CxOUT pin. The COUT bit (CMxCON<8>) reports the output state of the comparator, as determined by the relative values of Vin+ and Vin- and the CPOL bit (CMxCON<13>).

The CREF and CCH<1:0> bits (CMxCON<4> and <1:0>, respectively) configure the VIN+ and VIN- inputs to the comparator. The VIN+ pin can select from a dedicated analog input (CxINA) or the comparator voltage reference (CVREF or CVREF+). The VIN- pin can select from four sources: three other dedicated analog inputs (CxINB, CxINC or CxIND) or voltage reference (CVREF- or VBG/2). Taken together, this provides a total of eight input configurations for each comparator. (The CVREF and internal band gap options available to the user are solely determined by the comparator voltage reference module available on the microcontroller. Voltage reference options are controlled by the CVRCON register, discussed in **Section 20. “Comparator Voltage Reference Module”**.)

The EVPOL bits (CMxCON<7:6>) configure the event-detection logic to report changes to the output state of the comparator, which can in turn be used for event or interrupt generation. The options include event generation on rising state changes (low-to-high), falling state changes (high-to-low), and all state changes. When a configured event occurs, it is flagged by the CEVT bit (CMxCON<9>).

The CMSTAT register (Figure 46-2) serves as a convenient monitor for the status of all comparators; one CMSTAT register is implemented for the entire module. The CxOUT and CxEVT bits mirror the states of the corresponding bits in the CMxCON registers on a synchronous basis. In the CMSTAT register, all CxOUT and CxEVT bits are read-only, and cannot be changed. In addition, the CMIDL bit (CMSTAT<15>) determines how the comparator module as a whole operates when the microcontroller is in Idle mode.

Register 46-1: CMxCON: Comparator x Control Registers (Comparators 1 Through n)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **CON:** Comparator Enable bit
 1 = Comparator is enabled
 0 = Comparator is disabled

- bit 14 **COE:** Comparator Output Enable bit
 1 = Comparator output is present on the CxOUT pin
 0 = Comparator output is internal only

- bit 13 **CPOL:** Comparator Output Polarity Select bit
 1 = Comparator output is inverted
 0 = Comparator output is not inverted

- bit 12-10 **Unimplemented:** Read as '0'

- bit 9 **CEVT:** Comparator Event bit
 1 = Comparator event defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
 0 = Comparator event has not occurred

- bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
 1 = $V_{IN+} < V_{IN-}$
 0 = $V_{IN+} > V_{IN-}$

- bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
 10 = Trigger/event/interrupt generated on transition of the comparator output:
 If CPOL = 0 (non-inverted polarity):
 High-to-low transition only.
 If CPOL = 1 (inverted polarity):
 Low-to-high transition only.
 01 = Trigger/Event/Interrupt generated on transition of comparator output:
 If CPOL = 0 (non-inverted polarity):
 Low-to-high transition only.
 If CPOL = 1 (inverted polarity):
 High-to-low transition only.
 00 = Trigger/event/interrupt generation is disabled

- bit 5 **Unimplemented:** Read as '0'

Note 1: The use of either CVREF or CVREF+ for CREF options, and VBG/2 or CVREF- for CCH<1:0> options, are device-specific and not selectable by the user. Refer to the device data sheet for specific information.

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Register 46-1: CMxCON: Comparator x Control Registers (Comparators 1 Through n) (Continued)

- bit 4 **CREF:** Comparator Reference Select bits (non-inverting input)
 1 = Non-inverting input connects to internal CVREF or CVREF+ source⁽¹⁾
 0 = Non-inverting input connects to CXINA pin
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
 11 = Inverting input of comparator connects to internal VBG/2 or CVREF- source⁽¹⁾
 10 = Inverting input of comparator connects to CXIND pin
 01 = Inverting input of comparator connects to CXINC pin
 00 = Inverting input of comparator connects to CXINB pin

Note 1: The use of either CVREF or CVREF+ for CREF options, and VBG/2 or CVREF- for CCH<1:0> options, are device-specific and not selectable by the user. Refer to the device data sheet for specific information.

Register 46-2: CMSTAT: Comparator Module Status Register

R/W-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
CMIDL	—	C6EVT ⁽¹⁾	C5EVT ⁽¹⁾	C4EVT ⁽¹⁾	C3EVT ⁽¹⁾	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	C6OUT ⁽¹⁾	C5OUT ⁽¹⁾	C4OUT ⁽¹⁾	C3OUT ⁽¹⁾	C2OUT	C1OUT
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15 **CMIDL:** Comparator Stop in Idle Mode bit
 1 = Module does not generate interrupts in Idle mode, but is otherwise operational
 0 = Module continues normal operation in Idle mode
- bit 14 **Unimplemented:** Read as '0'
- bit 13-8 **CxEVT:** Comparator x Event Status bit (Comparators 1 through 6) (read-only)⁽¹⁾
 Shows the current event status of Comparator x (CMxCON<9>).
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **CxOUT:** Comparator x Output Status bit (Comparators 1 through 6) (read-only)⁽¹⁾
 Shows the current output of Comparator x (CMxCON<8>).

Note 1: Bits are only implemented when the corresponding number of comparators are present in the module. Refer to the specific device data sheet for more information. When the comparators are not present, these bits are unimplemented and read as '0'.

46.3 COMPARATOR OPERATION

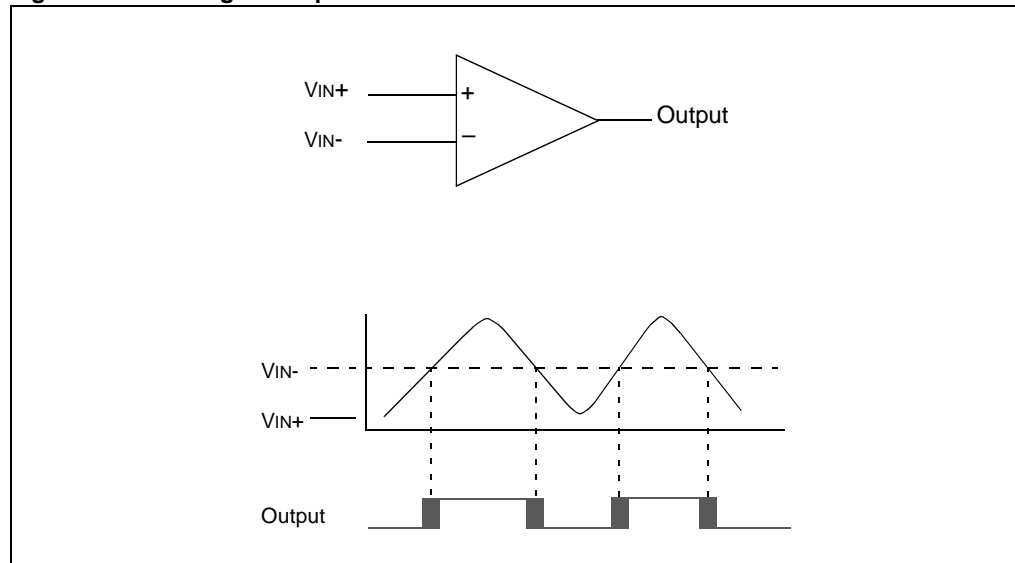
A single comparator is shown in Figure 46-3, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. When the analog input at V_{IN+} is greater than the analog input V_{IN-} , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 46-3 represent the uncertainty due to input offsets and response time.

46.3.1 Internal Reference Signals

Some applications require multiple comparators to operate from a common reference. The comparators allow the selection of an internally generated voltage reference, CV_{REF} , from the comparator voltage reference module. The internal reference is available to a comparator at its non-inverting input when the $CREF$ bit ($CMxCON<4>$) is set. On some PIC24F devices, an optional CV_{REF-} signal can be selected at the inverting input with the CCH bits ($CMxCON<1:0>$).

The voltage reference and its options are described in more detail in **Section 20. “Comparator Voltage Reference Module”**. For device-specific options, refer to the device data sheet.

Figure 46-3: Single Comparator



46.4 COMPARATOR RESPONSE TIME

Response time is the maximum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs (Refer to T_{set} , VR310, on the data sheet.) Otherwise, the maximum delay of the comparators should be used. Refer to T_{resp} on the data sheet for the particular part.

46.5 COMPARATOR OUTPUTS

The comparator outputs can be read from the CMxCON and CMSTAT registers. The COUT/CxOUT bits are read-only, as are the CxEVT bits in CMSTAT; the CEVT bit in each CMxCON register is both readable and writable.

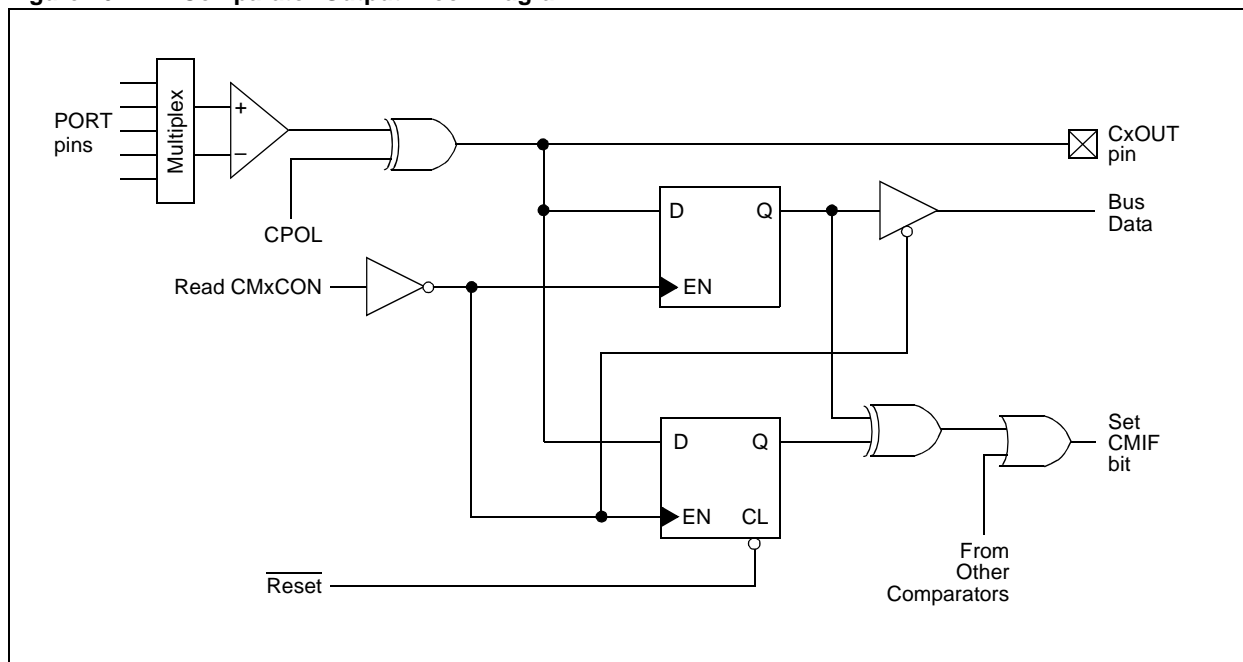
The comparator outputs may also be directly output to the I/O pins by setting the COE bit. When enabled, multiplexers in the output path of the I/O pins switch, and the unsynchronized output of the comparator appears on the CxOUT pin. Figure 46-4 shows the comparator output logic.

The polarity of the comparator output can be changed using the CPOL bit (CMxCON<13>); setting the bit inverts the digital output as defined in **Section 46.3 “Comparator Operation”**. This change carries through uniformly to the internal status indicator bit and the output pin, as well as to event detection logic.

The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the electrical specifications.

- Note 1:** When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
- 2:** Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

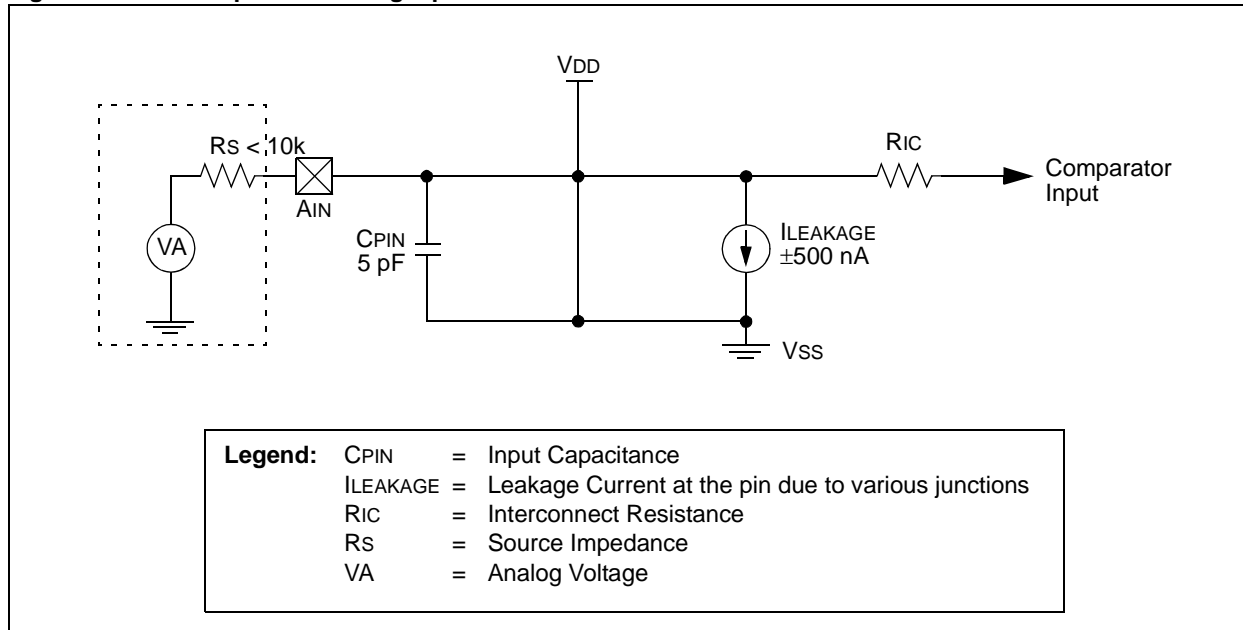
Figure 46-4: Comparator Output Block Diagram



46.6 ANALOG INPUT CONNECTION CONSIDERATIONS

A simplified circuit for an analog input is shown in Figure 46-5. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current. Refer to the device data sheet for input voltage limits.

Figure 46-5: Comparator Analog Input Model



46.7 COMPARATOR INTERRUPTS

The Comparator Interrupt Flag $CMIF$ ($IFS1 < 2 >$) is set whenever the Event flag of any comparator is set. The application can read $CEVT$ ($CMxCON < 9 >$) or the corresponding $CxEVT$ bit ($CMSTAT < 8 + x >$) to determine the actual source.

Note that the $CEVT$ bit is writable via the $CMxCON$ register. After event detection, hardware sets $CEVT$; it must be cleared in software to enable another operation. Both the $CMIF$ and $CEVT$ bits must be reset by clearing them in software.

If the $CMIE$ bit ($IEC1 < 2 >$) is cleared, an interrupt will not be generated; however, the $CMIF$ bit will still be set if an interrupt condition occurs. The user can clear the interrupt in the Interrupt Service Routine by clearing $CMIF$. See **Section 8. "Interrupts"** in this manual for more information.

46.8 CODE EXAMPLES

The following code examples show a typical sequence for initializing and configuring a detection event for an analog comparator. While these examples only discuss a single comparator, operations for several comparators are very similar.

46.8.1 Initialization

The initialization sequence in Example 46-1 configures one unit (C2) in the comparator module with its output enabled and inverted. The C2IN- terminal is connected to V_{BG}/2 (nominally, 600 mV) and the C2IN+ terminal is fed from the C2INA pin. The delay used in the example is based on an 8 MHz oscillator.

Example 46-1: Comparator Configuration

```
// PIC24F256GB110 Comparator C2 Initialization Example
// Pin 22: C2INA.

#define C1OUT_IO 1 // C1 OUT # for Pin MUX Table
#define C2OUT_IO 2 // C2 OUT # for Pin MUX Table
#define C3OUT_IO 36 // C3 OUT # for Pin MUX Table

TRISBbits.TRISB3 = 1; // Disable Digital Output on port pin
AD1PCFGbits.PCFG3 = 0; // Set input to Analog

IEC1bits.CMIE = 0; // IE Off so no interrupt occurs from set-up

CM2CONbits.COE = 1; // Enable output pin
CM2CONbits.CPOL = 1; // Invert sense. +In High ==> Out Low
CM2CONbits.EVPOL = 0; // No event detection
CM2CONbits.CREF = 0; // +IN is C2INA Pin
CM2CONbits.CH = 3; // -IN is Vbg/2 ~ = 0.60 V
CM2CONbits.CON = 1; // Turn Comparator ON

IFS1bits.CMIF = 0; // Clear IF after set-up

// Assign C2OUT to desired RP pin.
// (See Sec 12 I/O Ports with PPS.)

asm volatile("repeat #40"); //Delay 10us
Nop();
```

46.8.2 Event Capture

The example in Example 46-2 shows the use of the comparator's event detection logic. Note that the EVPOL bits select the direction of the edge to be detected, and provides an option for choosing both edges, thus detecting any change. Furthermore, the CPOL bit switches polarity before the edge detector.

Although status is checked in a simple while loop here, it would most often be found in an Interrupt Service Routine (ISR). In the ISR, the CMSTAT register gives visibility of all comparators simultaneously. However, CMSTAT flags are read-only, and the detect bits must be cleared in the individual CMxCON registers.

Example 46-2: Comparator Event Detection

```
// PIC24F256GB110 Comparator C1 Event Example
// Pin 21: C1INB.

#define C1EVT 0X0100 // Event flag in CMSTAT Module Status Reg
#define C2EVT 0X0200 // Event flag in CMSTAT Module Status Reg
#define C3EVT 0X0400 // Event flag in CMSTAT Module Status Reg
#define C1OUT 0X0001 // Output flag in CMSTAT Module Status Reg
#define C2OUT 0X0002 // Output flag in CMSTAT Module Status Reg
#define C3OUT 0X0004 // Output flag in CMSTAT Module Status Reg

unsigned int eventCount = 0;

TRISBbits.TRISB4 = 1; // Disable Digital Output on port pin
AD1PCFGbits.PCFG4 = 0; // Set input to Analog

IEC1bits.CMIE = 0; // IE Off so no interrupt occurs from setup

CM1CONbits.COE = 0; // Disable output pin
CM1CONbits.CPOL = 0; // Standard sense. +In High ==> Out High
CM1CONbits.EVPOL = 2; // Event detected on output edge falling
CM1CONbits.CREF = 1; // +IN is internal CVRef
CM1CONbits.CCH = 0; // -IN is C1INB Pin
CM1CONbits.CON = 1; // Turn Comparator ON

CVRCON = 0x88; // CVRef = (1/2) * (AVdd - AVss)

CM1CONbits.CEVT = 0;
IFS1bits.CMIF = 0; // Clear IF after set-up

// When C1INB RISES above AVdd/2,
// C1OUT falls & edge is counted.
// Loop forever
while (1)
{
    if (CMSTAT & C1EVT) // Check C1EVT bit
    {
        eventCount++; // Count edges for whoever uses them
                    // Must use Control Register to clear flag.
                    // Status is read-only.

        CM1CONbits.CEVT = 0;
    }
}
```

46.9 OPERATION DURING SLEEP AND IDLE MODES

46.9.1 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake-up the device from Sleep mode, when enabled. Each operational comparator will consume additional current, as shown in the comparator specifications.

To minimize power consumption while in Sleep mode, turn off all comparators by clearing the CON bits ($CMxCON<15> = 0$), before entering Sleep. If the device wakes up from Sleep, the contents of the $CMxCON$ registers are not affected. See **Section 10. “Power-Saving Features”** in this manual for additional information on Sleep.

46.9.2 Comparator Operation During Idle

When a comparator is active and the device is placed in Idle mode, the comparator remains active and interrupts are generated, if enabled, and $CMIDL = 0$ ($CMCON<15>$). If it is desired for the comparators to operate in Idle mode without generating interrupts, set the $CMIDL$ bit ($CMSTAT<15>$). See **Section 10. “Power-Saving Features”** in this manual for more information on Idle.

46.10 EFFECTS OF A RESET

A device Reset forces the $CMxCON$ registers to their Reset state, causing the comparators to be turned off ($CON = 0$). However, the input pins multiplexed with analog input sources are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the $ADxPCFG$ or $ANSx$ registers, depending on the device. Therefore, device current is minimized when analog inputs are present at Reset time.

46.11 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator module are:

Title	Application Note #
Resistance and Capacitance Meter Using a PIC16C622	AN611
Make a Delta-Sigma Converter Using a Microcontroller's Analog Comparator Module	AN700
A Comparator Based Slope ADC	AN863
Oscillator Circuits for RTD Temperature Sensors	AN895
Temperature Measurement Circuits for Embedded Applications	AN929
Analog Sensor Conditioning Circuits – An Overview	AN990

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

46.12 REVISION HISTORY

Revision A (January 2010)

This is the initial released revision of this document.